

Evolution, Design, and Implementation of a Modular Portable Lab Kit for Logic Design

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Abstract—Introduction to Logic Design is a course required for many engineering majors. It has a laboratory component that requires access to a Digital Logic Lab to test the designed logic circuits. The creation of an on-line session of the course required that the students not need to come to campus. This paper presents the evolution and design of a tether-less lab kit that is modular, low-cost, light-weight and built by the students as part of the class; and analyses results of the impact of this change in improving student experience and success are presented.

Keywords - Remote Laboratories, STEM Education, on-line Classes, on-line Laboratories, Virtual Laboratories.

I. INTRODUCTION

Engineering lab courses place demands on the university and students. The university staffs the laboratories to provide students better access to equipment, components and materials needed to complete and debug their experiments. This requires seats in physical laboratories. Universities are dealing with larger classes and increased pressure to provide on-line courses that provide access to remote students that may not be able to come to campus during the hours the lab is opened or staffed. Due to the exigency of the students daily lives, conflicts arise with location and availability. This paper presents methodologies to address these issues.

II. PROVIDING ACCESS TO THE PHYSICAL LAB

To maximize the use and staffing of physical space for laboratories the Department of Computer and Electrical Engineering and Computer Science (CEECS) in Florida Atlantic University's (FAU) College of Engineering and Computer Science implemented a policy of shared laboratories: each physical laboratory was designed to support at least 2 different lab courses. The CEECS combined the lab spaces for improved supervision and Lab support. The logic design lab was combined with the microprocessor and embedded systems labs; and the introductory classes of Fundamentals of Engineering share two labs, depending on the lesson plan, with the Senior Design lab, or with the Electronic Circuits I and II lab. Additionally, to provide added supervision and access to materials and components, the laboratory support and repair office shares a glass wall with 24x7 all purpose, general access laboratory with two fully equipped lab benches and a stock room with general

electronic components supply cabinets and wire. This permits the lab manager to serve students requesting expensive components, while supervising the general lab.

Figures 1-3 illustrates the floor plans and pictures of the Logic/Microprocessor/Embedded lab, the lab managers office and general access lab.

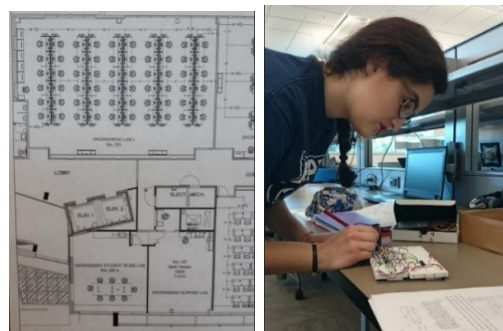


Fig. 1. (a) Floor plan (b) Student in lab with new lab kit

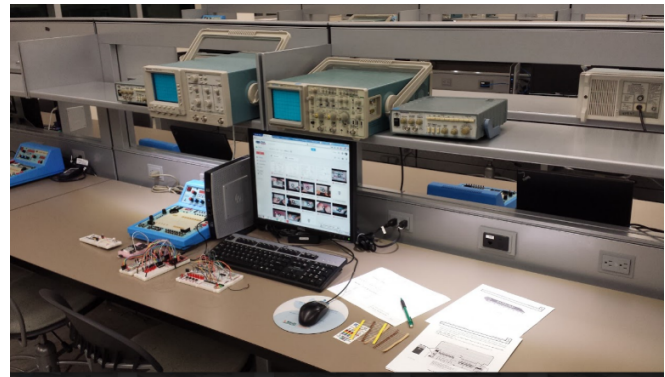


Fig. 2. Logic / Microprocessor / Embedded Lab setup (60 seats)

The building and the labs are equipped with magnetic card readers. Each employee, faculty and student are assigned an identification card with magnetic strips. At the beginning of each semester, all engineering students are granted 24x7 access to the physical laboratories associated with their courses, general study area, and the building.

Lab assistants (Teaching Assistants - TAs) are cross trained to assist and grade the labs for the courses assigned to their

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Fig. 3. View From Lab Manger's Office to the General Student Lab

laboratory. This allows two to three times the number of hours of supervision. Students work on the lab experiment or circuit during their own time and get their labs graded during the TAs scheduled coverage. The Logic / Microprocessor / Embedded lab was staffed with 6 lab assistants for approximately 60 hours per week: 8 to 10 hours per day, Monday through Saturday. A total of 430 students utilize this lab any given term: 200 Introduction to Logic Design students in 3 classes, 180 Introduction to Microprocessor Systems students in 3 classes, plus 50 Introduction to Embedded Systems Design students in 1 class. The lab assignments grades are recorded in a shared spreadsheet on a Google drive with access given to the professors of the classes and the lab assistants. One of the lab assistants is given the title of Super TA to oversee the lab assistants. One of the professors supervises the Super TA and oversees the common Lab Manual for each course. The Lab Manager orders all components and assembles the student lab kits with the assistance of the TAs. Originally, labs were due on Saturdays. Experience showed that was a suboptimal choice due to the heavy usage on Saturday. The optimal due dates are synchronized with the class meeting days.

III. MEETING THE NEEDS OF COMMUTER AND ON-LINE STUDENTS

Only 12% of FAU students live in university housing, the rest commute. FAU services a quad-county area that covers over 200 miles by 50 miles. There is an increased demand to provide more engineering courses on-line. Lab Engineering courses need to provide a lab kit that both commuter and on-line students can use at home to build and test their logic circuits.

Additionally, the on-line students require a process to assist and grade their labs without having to come on campus. The need for development of remote, virtual and mobile labs has led the Education Society of the Institute of Electrical and Electronics Engineers (IEEE) to form a working group to develop standards for P1876 Networked Smart Learning Objects for on-line Laboratories[1]. There are many different models that can be used for mobile and on-line laboratories[2].

IV. THE ORIGINAL DIGITAL LOGIC LAB

The digital logic design has been defined by IEEE and ACM societies as one of core areas.[1] Many universities use digital logic design as the gateway course to undergraduate computer science and computer & electrical engineering. In this section we will focus on the impact of developing a mobile lab for this course. The planned roll-out for one section of the Introduction to Logic Design was Spring 2016, it was the first engineering lab course at FAU to be converted to completely on-line delivery. As a result in Fall 2014 portable lab kits started to be developed by one of the professors.

The physical lab in Figure: 1a was equipped with 60 units of the IDL-800A Digital Lab, Figure: 4, the \$800 units weighs 4kg, with logic switches & indicators, signal generator, power supplies, and a volt meter. Other available equipment includes oscilloscopes and laptops. All this equipment requires line power to operate. Our goal was to develop a stand-alone, low cost, tether-less lab that the students could build themselves.



Fig. 4. Digital Lab and Logic Trainer

The logic lab manual contained six labs:

- 1) Equivalence lab: Build 2 NOT-AND-OR circuits and show they are equivalent by comparing outputs and truth tables.
- 2) Arithmetic lab: Build a 1-bit full adder using all NAND gates and expand to 5-bit adder utilizing a 4-bit adder chip.
- 3) Decoders lab: Build a circuit using 2 3-to-8 decoders and NAND chips to implement a 4 variable Boolean Algebra expression.
- 4) Sequential lab: Trace a sequential circuit and verify output by building the circuit and comparing the output.
- 5) Sequential lab: Build a Moore circuit that implements a Finite State Machine, utilizing J-K flip flops and NANDs.
- 6) 2-digit BCD counter: Build an up-down 00-99 counter that displays output on a dual 7-segment display utilizing BCD counters, multiplexer, NAND gates and a clock.

The original lab kit utilizing the Digital Lab cost \$11.99, Table I. Contained one breadboard, a combination of ICs

from the 7400 family and wire. Students provided wire cutter-strippers, and a needle-nose plier.

V. FIRST PORTABLE LOGIC LAB KIT (PLLK1)

Current Logic Labs were outdated and under-serving the engineering community. The CEECS department decided it was necessary to research and develop an intuitive Portable Logic Training Lab for use by students whether on or off campus that could also take advantage of options vis--vis the Internet for remote access.

In Fall 2014 B. Alahalabi & P. Pastran implemented a low-cost portable lab kit that Logic Design students could build themselves and use to experiment and test anywhere. Students, regardless of prior electronics experience, can assemble the Portable Logic Lab Kit (PLLK). The PLLK allows the student to power, test, and control their logic lab assignments for an entire semester.

In the first version of the PLLK a minimal of components were included to provide inputs, outputs and power to the original kit. This added \$8.57 of cost, with the total cost of the first prototype at \$21.99, Table: I. It was tested with one of three sections of the Logic Design course. As students from other classes observed the students with the portable kits, they requesting that it be expanded to all the sections.

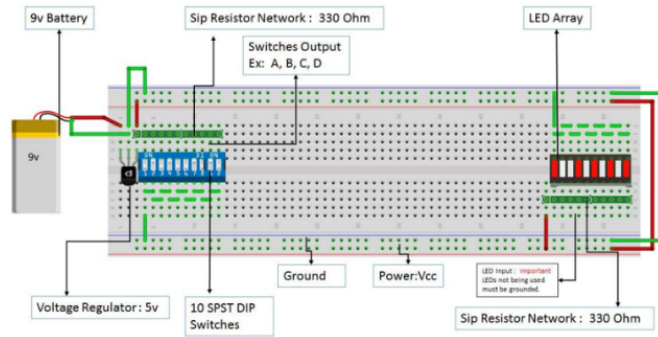


Fig. 5. Wiring diagram [11] for the PLLK1: By P. Pastran

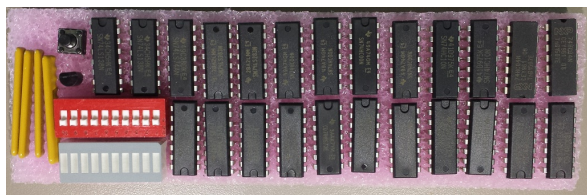


Fig. 6. Lab kit components distributed with breadboard and wire

The PLLK1 wiring diagram is shown in Figure: 5, it is powered by a 9V battery, a 5V voltage regulator, a 10 unit DIP switch for input, a push button switch to simulate the clock, an array of 8 Light Emitting Diodes (LEDs) for output, and an 8 resistor resistor network. This made the lab kit mobile, shown in Figure: 6.

TABLE I

PARTS LIST FOR LOGIC TRAINER & PORTABLE KIT (PLLK1)

pn	desc	quan	each	Lab	PLLK1
SN74HC00N	Quad 2in NAND	4	\$0.18	\$0.72	\$0.72
74HC04N	Hex Inverter	2	\$0.26	\$0.52	\$0.52
CD74HC08E	Quad 2in AND	2	\$0.18	\$0.36	\$0.36
SN74HC10N	Triple 3in NAND	2	\$0.18	\$0.36	\$0.36
SN74HC20N	Dual 4in NAND	2	\$0.19	\$0.38	\$0.38
CD74HC32E	Quad 2in OR	1	\$0.18	\$0.18	\$0.18
CD74HC73E	Dual JK Flip Flop	2	\$0.42	\$0.84	\$0.84
SN74LS74AN	Dual D Flip Flop	1	\$0.37	\$0.37	\$0.37
SN74LS138N	3:8 Demultiplexer - Decoder	2	\$0.34	\$0.68	\$0.68
SN74HC157N	Quad 2:4 Multiplexer - Encoder	2	\$0.76	\$1.52	\$1.52
SN74LS283N	4bit Adder	2	\$0.34	\$0.68	\$0.68
CD4510BE	BCD UP-DOWN COUNTER	2	\$0.28	\$0.56	\$0.56
4611X-101-331LF	BOURNS Resistor Network 10x 330Ohm	4	\$0.46		\$1.84
703-0190	LED Bar Graph Array 10	1	\$2.37		\$2.37
LM78L05ACZ	5v Voltregulator - 100mA	1	\$0.15		\$0.15
78B10T	DIP Switch; SPST; Raised Slide; 10 Position	1	\$3.15		\$3.15
HH-3449	9v battery clip w wire	1	\$0.90		\$0.90
	Breadboard 830points	1	\$3.75	\$3.75	\$3.75
	Packaging: Labor; Anti-static Foam; Bags	1	\$2.50	\$2.50	\$2.50
	Total			\$13.42	\$21.99

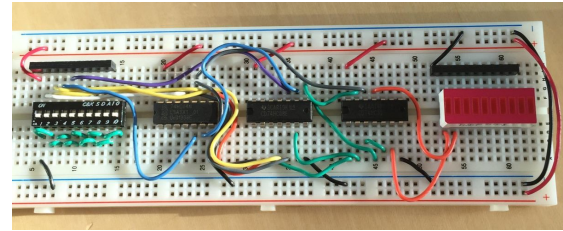


Fig. 7. PLLK1 Lab 1, Gate Reduction & Equivalence: Student Built

As a method to teach the difference of active high and active low, the switches were wired active low as a means of exploring the difference.

Students responded with enthusiastic feedback about the portable lab kit: they were to able make the mobile lab and spend time debugging their labs at home instead of the physical lab; this freed the lab stations to serve more students. While is is possible to fit all lab circuits on the one breadboard provided, lab #2 required exact placement of chips. The Arithmetic Lab, #2, utilized nearly every row, as shown in Figure: 16. The lesson of the difference between pull-up and pull-down resistors was eliminated because it confused students as part of their first experiment.

VI. SECOND PORTABLE LAB KIT (PLLK2)

Many of the features of the PLLK1 were carried over to PLLK2, albeit in component form and have the added advantage of returning the students to component level instruction. This not only reduced costs, it allows each student to personally understand the impact of each decision they make in circuit design.

The FAU Lab Manager provides instructional videos[12]-[26] that guide students as they move through the beginning logic assignments. The videos[12]-[26] cover every aspect from demonstrating the basic assembly and operation of a breadboard to wire stripping to IC pin straightening to explaining the function of each component and how to assemble the Logic Labs infrastructure step-by-step including exact placement of each part. This was necessary as many students had never seen a breadboard and/or taken Physics

2 or Circuits 1 and were critically unprepared in electronics and/or the use of breadboards.

The PLLK2 Includes: a robust battery-operated power supply, reverse polarity protection for the logic buses, LED status indicators, more DIP-switches, more push button switches, Tri-State logic probe, dual 7-segment display, and dual square wave oscillators. To keep the portable lab kit cost down, \$20.15 Table II. The resistor array and LED arrays were substituted for individual resistors and LEDs, Figures: 6 & 8.

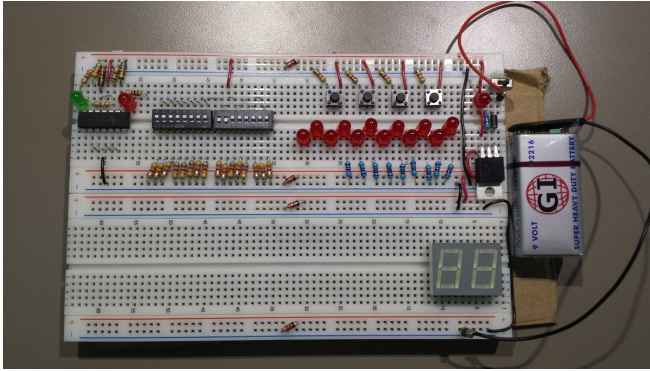


Fig. 8. Wired 2nd Portable Logic Lab Kit (PLLK2)

The cost of kitting was eliminated by utilizing all TAs assigned to departmental courses to assemble and package the kits the first week of classes, Figures: 9 - 11. The TAs build over 750 kits for all the classes with labs: Logic Design Microprocessors, Electronics Labs 1 & 2, Senior Design. They also build kits for the special offering classes with labs: Electromagnetic Compatibility, Summer Camp High School Electronics Lab, Hack-A-Thon, among others.



Fig. 9. A TA putting the ICs into anti-static foam



Fig. 10. The assembly line for small parts



Fig. 11. A TA putting the Logic Kits together

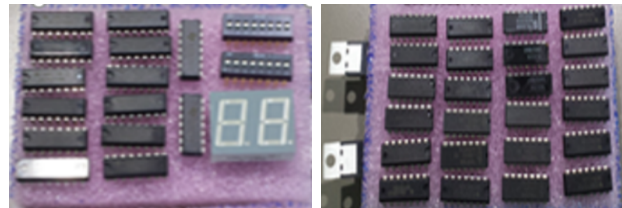


Fig. 12. Lab kit components distributed with breadboard and wire

To avoid having to mail replacement components to on-line students and to avoid component failure, we examined methods to "harden" the kit. Eliminating issues due to incorrect wiring, a diode protects against incorrect polarity of the 5V regulator (LM7805). Zener diodes prevent issues caused by connecting the 9V battery to the 5V bus, or worse connecting the 9V backwards to the 5V bus. Capacitors were added to maintain a steadier 5V signal. To reduce student anxiety due to the increased analog components a set of videos[12]-[26] guides them step-by-step through the building of the infrastructure section of breadboard and testing of the NOT, AND, OR, and NAND chips as preparation to their orientation lab.

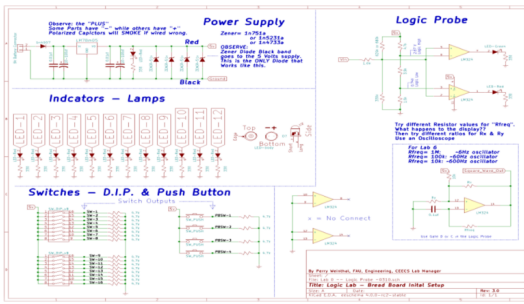


Fig. 13. Schematic for PLLK2, shown larger in the Appendix

TABLE II

PARTS LIST FOR LOGIC TRAINER & PORTABLE KIT (PLLK2)

quan	part number	Description	each	ext
6	7400	Quad 2in NAND	\$0.177	\$1.06
3	7404	Hex Inverter	\$0.177	\$0.53
3	7408	Quad 2in AND	\$0.146	\$0.44
3	7410	Triple 3in NAND	\$0.177	\$0.53
3	7420	Dual 4in NAND	\$0.063	\$0.19
2	7432	Quad 2in OR	\$0.099	\$0.20
2	7474	Dual D Flip Flop	\$0.130	\$0.26
2	74109	Dual J K Flip Flop	\$0.242	\$0.48
3	74138	3-8 Demultiplexer / Decoder	\$0.212	\$0.64
2	74157	Quad 2-4 Mux / Encoder	\$0.351	\$0.70
1	74283	4bit Adder	\$0.212	\$0.21
3	cd4510	Pre. BCD Up-Down Counter	\$0.280	\$0.84
2	cd4543	BCD 7seg. CA or CC	\$0.260	\$0.52
2	LM324	Op-Amp Quad	\$0.193	\$0.39
2	78m05	5v Volt Reg. 500mA TO-220	\$0.166	\$0.33
1	LDDHTA514RI	LED DUAL 7seg 2Anodes	\$0.970	\$0.97
2	SW.DIP-08	Dip SW-08	\$0.800	\$1.60
6	PB.SW-n.o.	SW TACT SPST-NO 50mA	\$0.160	\$0.96
1	9V Bat Conn	9v clip w 8 wire tinned	\$0.170	\$0.17
20	LED.Red	LED Red 5mm	\$0.020	\$0.40
2	LED.Green	LED Green 5mm	\$0.020	\$0.04
2	LED.Yellow	LED Yellow 5mm	\$0.020	\$0.04
1	LED.Blue	LED Blue 5mm	\$0.030	\$0.03
2	0.1uF Cap	0.1 uf 20% 50v cap	\$0.017	\$0.03
30	330 Ohm 0.25W Res. @ 5%	Orange Orange Brown Gold	\$0.008	\$0.24
2	1.0k 0.25W Resistor 5%	Brown Black Red Gold	\$0.013	\$0.03
2	1.5k 0.25W Resistor 5%	Brown Green Red Gold	\$0.013	\$0.03
2	3.9k 0.25W Resistor 5%	Orange White Red Gold	\$0.013	\$0.03
30	4.7k 0.25W Resistor 5%	Yellow Violet Red Gold	\$0.008	\$0.24
5	10k 0.25W Resistor 5%	Brown Black Orange Gold	\$0.013	\$0.07
2	330k 0.25W Resistor 5%	Orange Orange Yellow Gold	\$0.013	\$0.03
2	620k or 680k 0.25W 5%	Blue (Red or Gray) Yellow Gold	\$0.013	\$0.03
2	1M 0.25W Resistor 5%	Brown Black Green Gold	\$0.030	\$0.06
6	1n751a	5.1v Zener Diode	\$0.019	\$0.11
2	1n4007	1amp Diode	\$0.025	\$0.020
1	PBSW0.1	Slide Switch SPST	\$0.020	\$0.020
2		Breadboard 830points	\$3.750	\$7.50
1		Anti-Static Mat	\$0.020	\$0.02
1		Anti-Static Bag	\$0.142	\$0.14
		Kit Total		\$20.15

Wiring the 2nd Portable Logic Lab Kit (PLLK2), Figure 8. is expected to be completed by week 3 of the course. The dual 7-segment display is wired later. Schematics, Figure 13, we provided to the students to guide their building in conjunction with the step-by-step videos[12]-[26]. Extra ICs were provided in case of damage for both the on-line and live lecture classes, shown in Figure 12.

The analog components were not discussed in detail as part of the lecture class, but their functionality and detailed wiring was explained in the videos[12]-[26]. The majority of the students were able to wire the lab kit (without the 7-segment display and driver) in time for lab orientation by the 3rd week of class. Typical build time is ~10 hours. Those that had not completed their platform, wired their Lab#1 powered by the Digital Lab Trainer, Figure 4.

During the orientation the class was split into 3 groups. One group went to the physical lab orientation to wire their first example circuit. A second group went to soldering or-

ientation where they learned to solder by soldering solid leads to their 9V battery clip. We ordered ones without leads for the second prototype to reduce cost and take the opportunity to make sure all the students knew how to solder and review the Lab Safety Rules, on-line students are provided with pre-soldered 9V leads. The third group went to the computer lab where they learned how to use the circuit simulator Altera Quartus II, Figure 15. They completed the schematic for their sample circuit, and generate the vector waveform output for comparison with their truth table. Each group cycled through the three activities to complete orientation.

The PLLK2 was Logic Probe tested with students in one section of the course. It was made optional, all students completed the platform by the 4th week of class. The student feedback from the PLLK2 build was very positive. Students achieved a mastery and confidence not experienced in prior semesters. They were able to spend more time on their own experimenting with the kits, some began designing their own lab experiments.

The PLLK2 parts list, Table II, contains simpler, cheaper, and more durable parts; avoiding the issues caused by lack of parts knowledge experienced by many of the students. The PLLK2 provides 50% more spare parts, doubles the total available breadboard size and includes a Tri-State logic probe for increased confidence while debugging, (Low=Red, High=Green, Off=Un-Connected), Figure 14.

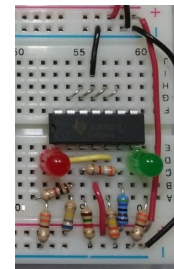


Fig. 14. PLLK2 Tri-State Logic Probe

To enhance the experience, students were required to perform Logic Simulation (using Quartus 2 [10]) for each lab, Figure 15.

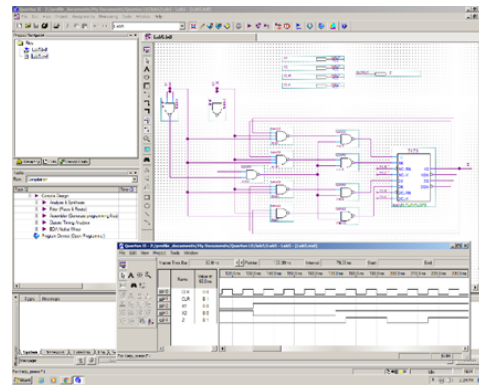


Fig. 15. Altera's Quartus 2 [10]

VII. DEMONSTRATIONS OF STUDENT BUILT LABS

When the students successfully complete labs they are often elated, we are often bewildered that the circuits are functional.

Using the PLLK1: A Full Adder built on a single breadboard, no extra work space, Figure 16.

Using the PLLK2: Lab1 Equivalent Equations Evaluation, Figure 17.

Using the PLLK2: The culmination of the labs: Lab 6 A Programmable Up/ Down 2 Digit Counter, Figure 18.

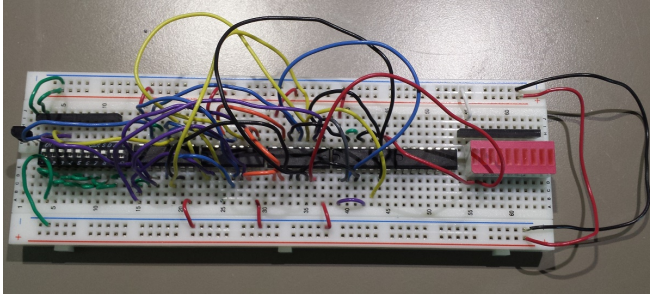


Fig. 16. PLLK1- Lab2 Full Adder: Student Built. Notice Lack of space

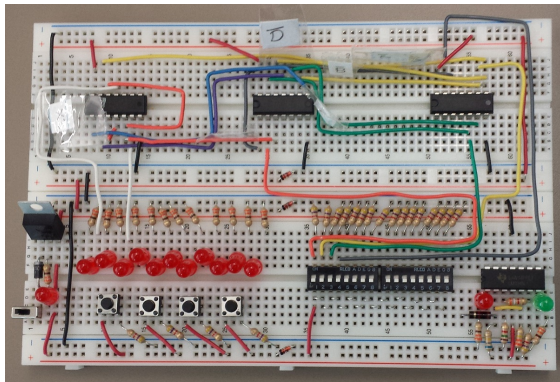


Fig. 17. PLLK2 Lab 1: Student Built

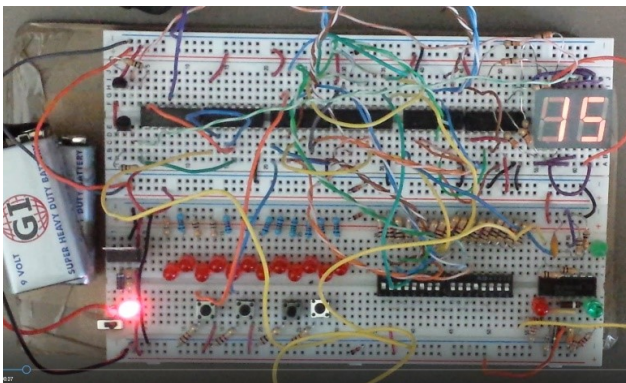


Fig. 18. The Final Project Lab 6: Student Built

VIII. RESULTS

Students connected the 9v battery to the 74xx chips directly causing them to fail. Adding Zener diodes across

each power bus shunts backwards connections and voltage overloads.

The use of SIP Resistor Networks & LED bar graph while space saving was a source of confusion for nearly all students, Figure 19. They are complex parts to students who lack an understanding of their construction and are expensive \$0.46 ea, vs an equivalent of \$0.08, Tables I & II. Additionally, the SIP Resistor Networks were prone to cracking failure resulting from improper handling.

The issues with the PLLK1 range from: no spare parts, the 7473 dual JK Flip-Flop chip, the 5V regulator, the SIP Resistor Networks, the push button switches and no spare room on the single breadboard. The 7473 was prone to incorrect wiring because it had a different power and ground pins than the other chips used in the kit. The LM78L05, 5V @ 100mA, voltage regulator was prone to being inserted backwards in addition to being significantly underrated for the load, turning on all 10 DIP switches would draw 150mA. The SIP Resistor Networks would crack leading to hours of frustrating troubleshooting. The push button switches were curved to fit into a PCB and would "pop out" of the breadboard randomly, along with they generate a very "bouncy" signal.

LM7805 Face(L-R): TO-220=In-Gnd-Out, TO92=Out-Gnd-In

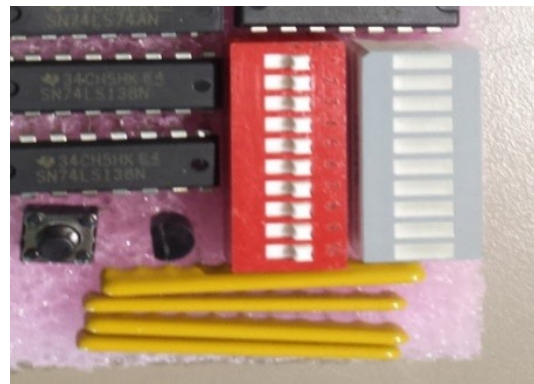


Fig. 19. PLLK1 Resistor Networks & Bar-graph Display

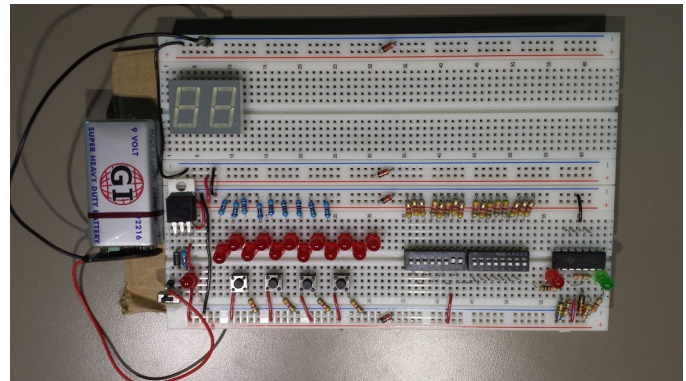


Fig. 20. PLLK2 Resistor & Indicator: Student Built

Changing to individual resistors & LEDs allowed the students to experience building the LED indicator circuits. The added benefit was a significant cost reduction (\$0.34 vs \$4.21, Tables I & II), allows purchasing additional parts: i.e at least one spare per part number, logic probe, and 7-segment display. Incorporating a Tri-State logic probe allows students to effectively troubleshoot their circuits and observe exactly how logic gates work, Figure 14. The substantial improvement in student confidence and success was worth the \$0.75 cost.

The Lab Manager was required to assist students on many occasions when the TAs were unable to resolve the issues. Some students plugged the 9V battery directly to the main 5V bus and destroyed multiple parts. The use of videos[12]-[26] to guide students on building the breadboard substantially improved the student success and reduced failures. A significant improvement was the result of several issues: Change & training of TA staffing, Videos[12]-[26], informing the students they were responsible for any damaged parts and the Lab Manager guest lecturing the first 2 weeks of class for 30 minutes.

On-line classes have been successfully accommodated using video conferencing and laboratory assignments can be graded by evaluating a video of the completed project uploaded by the student. There is a high class fill rate and retention.

IX. FUTURE IMPROVEMENTS

Include a proprietary Binary to Hexadecimal 7-Segment display driver, as there are no low-cost units currently on the market. This will enhance the students understanding of base conversions. The Logic Probe has been enhanced to indicate all three states visually: High (Blue), Low (Green) and Disconnected (Yellow). These will be discussed in a paper with these and other improvements for the 3rd version of the PLLK (PLLK3).

X. CONCLUSIONS

Portable Teaching Laboratories are a plausible low-cost solution for teaching on-site and remote / on-line classes. Students can achieve in-depth knowledge and develop skills when given reasonable supplemental materials to cover gaps in their knowledge of basic electronics. The availability of low cost tools and materials makes this possible.

APPENDIX

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PHOTO CREDITS

- 1a: By: FAU Planning
- 5: By: P. Pastran
- 1b: Used with Permission.
- 11: Used with Permission.
- All others Drawings, Pictures & Tables by the Author: C. P. Weinthal

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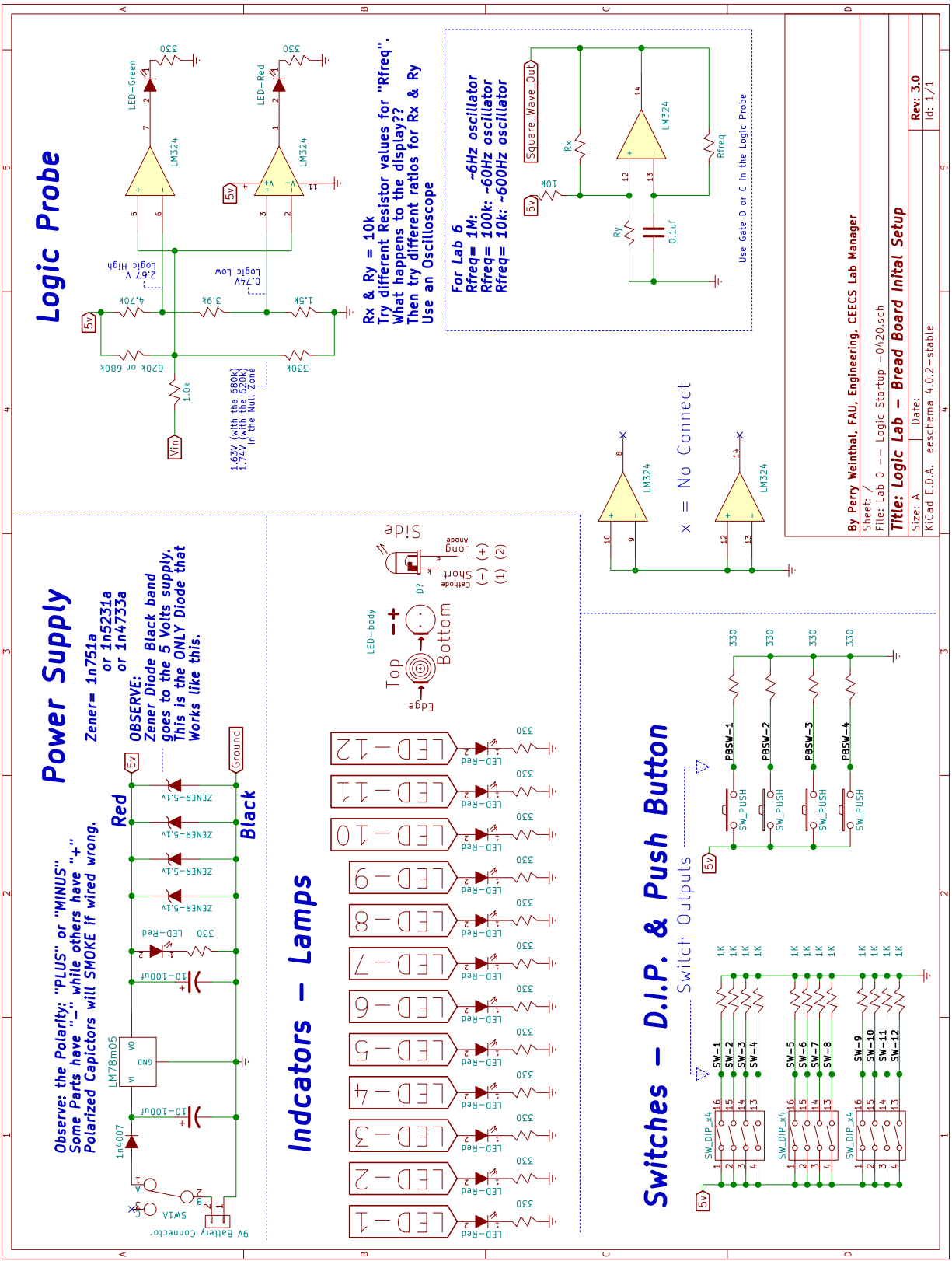


Fig. 21. Schematic for PLLK2

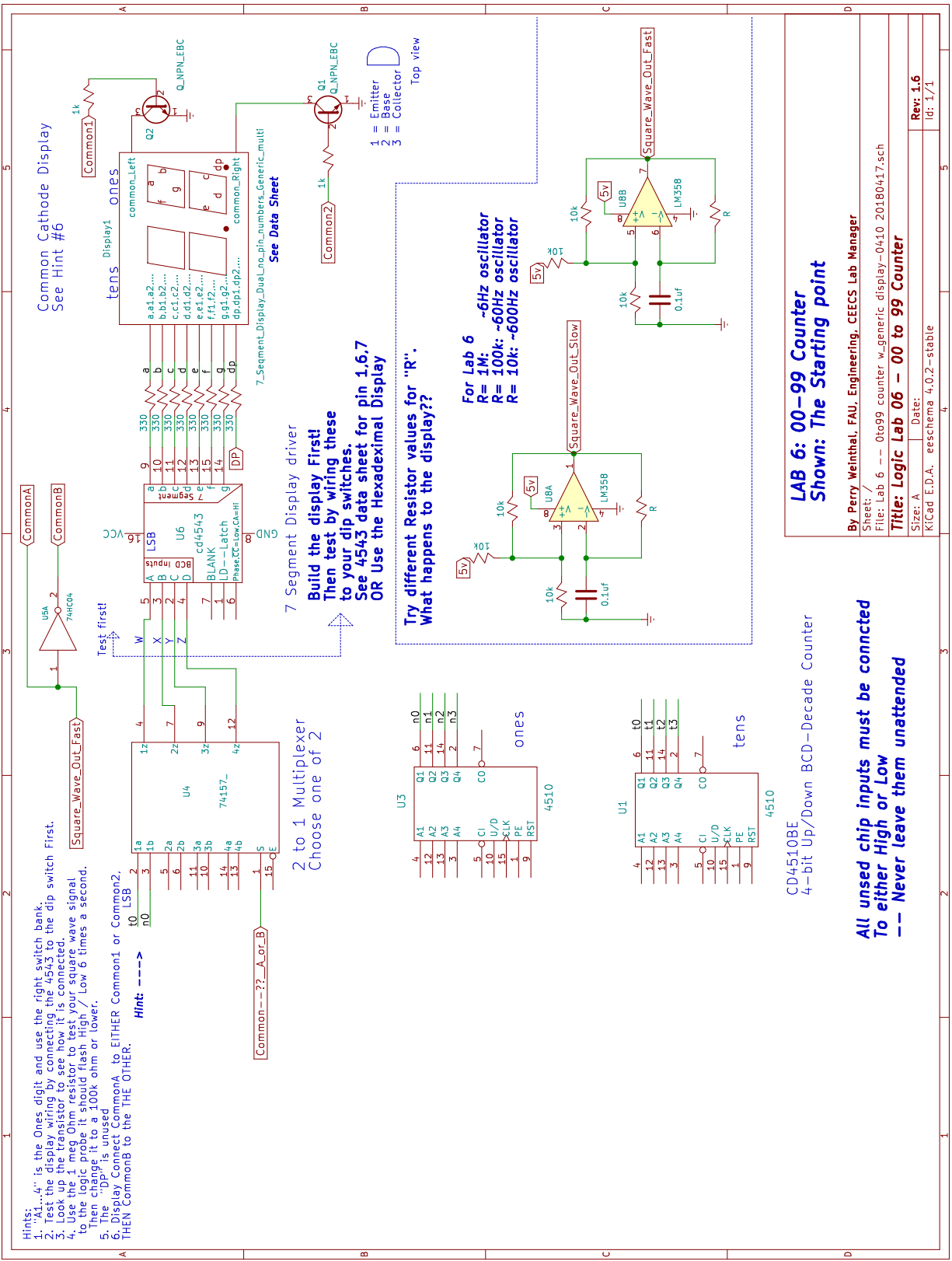


Fig. 22. Schematic for Lab6