Stiffness of YBCO thin films on LaAlO3 substrates for MEMS devices

Jorge Vargas
Universidad del Turabo, Gurabo, PR, USA, jvargas@suagm.edu

Yazan Hijazi
Universidad del Turabo, Gurabo, PR, USA, hijaziy@suagm.edu

Grover Larkins
Florida International University, Miami, FL, USA, grover.larkins@fiu.edu

ABSTRACT

A series of samples are being fabricated in YBCO thin films on LaAlO3 substrates to further use in (micro-electro-mechanical systems (MEMS) devices. Pulse laser deposition was found to be the best deposition process for the YBCO layer because of the ability to stoichiometrically transfer the composition of the target to the substrate. The LaAlO3 substrate has low loss tangent at low temperature, resulting in minimal dielectric loss in microwave circuits. Its dielectric constant of 24.5 provides a possibility of circuit miniaturization. The resolved examination of surface morphology will be presented using characterization techniques as x-ray diffraction, SEM and AFM. After the substrate is well covered by YBCO it is ready to implement the MEMS device layout patterning process. This device will be designed to be switched and its details will be also presented in this work. After the design process is complete the dc actuating part of the system is introduced and verified through simulations for an optimum switching device.

1. INTRODUCTION

MEMS devices and their applications have extended to different areas such as wireless communication which MEMS play an important role due to the benefits that MEM switches can offer over PIN-diode of FET counterpart [1] in terms of fabrication, cost operation linearity and functionality. In this work, we will focus on the fabrication of YBCO on LaAlO3 substrates using pulsed laser deposition to build optimum MEM switches. Therefore, characterization process is a key to resolve the morphology of the die surface using techniques as x-ray diffraction, SEM and AFM which will be presented. After the device characterization is done we will be set for the MEMS device layout patterning process. This device is designed to be switched operating at cryogenic temperatures.

2. FABRICATION

2.1 PULSED LASER DEPOSITION

Pulsed Laser Deposition was one of the first techniques used for the preparation of epitaxial HTS films [2] and also used for this work. A laser pulse heats a material target evaporating and creating a plume which is transported to the substrate [3]. The process can carry out oxygen depending on the pressure. The film produces large numbers of particles, which emanate from the ablation process. Several methods have been investigated to minimize the density of particles in a film, including time-of-flight methods to separate the heavy, slow particles from the faster atoms and ions [4]. Pulsed laser deposition of high-temperature superconductor materials provides high quality superconducting thin films because of the ability to stoichiometrically transfer the composition of the target to the deposited film [5]. In addition, the deposition rate is high and the apparatus is simple compared with the other deposition techniques [6]. A low temperature is set to avoid deterioration in the characteristics of under-layers already fabricated. For better optimization in the laser processing the temperature has to be distributed respectively. For this film deposition, laser wavelength is 532 nm.
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2.2 LAYOUT PATTERNING

After the substrate is well covered by YBCO it is ready for the layout patterning process. The photoresist that was used for imaging was AZ5214. This photoresist is used as a negative photoresist by imaging reversal process; this is done when a negative, high resolution wall profile is required [49]. This photoresist imaging process will provide adequate resolution since the dimensions of

the layout to be patterned were above 150µm. A double coat of photoresist spun on 3000 rpm for 30 seconds each and hotplate to produce a cleaner pattern and minimize film irregularities. In the preparation of BTO patches two layers are involved. The underlaying layer is a polymer (PMGI SF15) spun at 3000 rpm to a thickness of 4 μm. This layer is flood exposed to UV light for 4 minutes. This will provide solubility to ensure proper undercut for an ideal liftoff. The top layer is a coat of thin photoresist AZ5214 spun at 3000 rpm for 30 seconds. After coating the substrate is exposed for 3 minutes through the dielectric mask and submerged in a beaker with a 1:4 developer to DI water solution. After watching closely the development process of the patches and making sure that the undercut is well developed the substrate is moved to the RF magnetron sputtering system for BTO deposition and then bridge release.

3. Design

This section describes to the design process of this work. First of all, the design process starts by determining the dimensions required for the 50 Ω microstrip[45] transmission line. Second, MEMS switches are designed and characterized. Third, the device is designed to be switched and optimized using SONNET™ simulation[46] software. After the design process is complete the dc actuating part of the system is introduced and verified through simulations. Series capacitance contact MEMS[47] switches were selected for this project. The dimensions of the supported beam structure are shown in figure 3.1. The suspended membranes or bridges have a length L = 800 µm (approximately 5 x W), a width W = 169 µm and a gap height h_g = 2 µm.

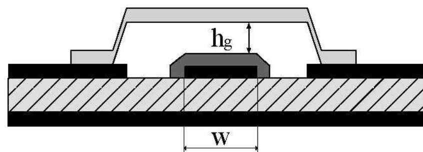

Figure 3.1: Series MEMS switch.

The superconductor was modeled as a conductor with a skin depth equivalent to the corresponding London penetration depth. SONNETTM is not capable of simulating mechanical movements, so the separate simulations were made for the “off” and “on” state. The suspended membrane in the “off” state or up position has a dielectric layer with □r = 1 (air) on top of the BaTiO3 patch. The height between the membrane and dielectric patch layer or air gap is approximately 2 µm. In the “on” state or down position, there is no air gap; therefore, the membrane is laying directly on the dielectric patch covering the transmission line. To actuate the gold membrane, a DC voltage is applied between the center conductor of the filter and the membrane. The resulting electrostatic force pulls the membrane down towards the filter transmission line.

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4. RESULTS

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References

[1] V. Sieracki, “Advances in MEMS for RF technology,” in *Proc. 2000 AOC Radar EW Conf. Session 2: Technol. Develop. Impact on Radar/ ESM*, Oct. 2000.

[2] Dijikkamp D., Venkatesan T., Wu X. D., Shaheen S. A., *Appl. Phys. Lett.* **51**, 619-621 (1987).

[3] Shen Z. Y., High Temperature Superconducting Microwave Circuits, Boston: Artech House, 3 (1995).

[4] Stoessel C. H., Bunshah R. F., Prakash S., and Fetterman H. R., J Supercond. 6, 1-17 (1993).

[5] Nakamiya T., Ikegami T., and Ebihara K., IEEE Trans. Appl. Supercond., 3, 1057-1060 (1993).

[6] Wu X., Dijkkamp D., Ogale S., Inam A., Chase E., Miceli P., Chan C., Tarascon J., and Venkatesan T., Appl. Phys. Lett. 51, 861-863 (1987).

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