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Electronic Work Bench and PSpice can be used for Design Extensions along with the Simulations

Subbarao V. Wunnava, PhD
Professor, Florida International University, Miami, Florida, USA, subbarao@fiu.edu

Temitope Marcus, P.E.
Research Associate,Positi Florida International University, Miami, Florida, USA, tmarc001@fiu.edu

Rafael Romero
Research Assistant, Florida International University, Miami, Florida, USA, rrome003@fiu.edu

Malcolm Heimer, PhDIng.
Associate Professor, Florida International University, Miami, Florida, USA, heimerm@fiu.edu

Abstract
The design ofA brief abstract of the research work not more than 200 words in length should be typed here. Must include a statement of relevance, the main electronic systems is becoming highly complex given the integrated nature of these systems. The use of a top-down design methodology is highly prevalent among designers given the availability of a diverse set of system level design tools. Such design tools include VHDL, Verilog, or SystemC just to name a few. These tools allow for the modeling and simulation of a system at different levels (system, register transfer, and component) of abstraction. However, to model or simulate an electronic circuit at the component level, simulation platforms such as PSpice and Electronic Workbench MultiSim are better suited for this type of simulation. At Florida International University, investigations were carried out using PSpice and the Electronic Workbench MultiSim to assess the feasibility of incorporating system level design capabilities into these simulation platforms. This paper will present the results of these investigations, using specific case studies involving analog, and digital circuits of different levels of complexity. Also, the authors will present and discuss the interface schemes between the traditional simulation packages such as the PSpice and the Workbench MultiSim, and the higher level abstraction languages such as the VHDL.objective, the scope of word to be presented, and most significant findings. Do not include figures, tables or illustrations in this section. (Times New Roman Font, Size 11pt, Single spacing, justified).

Keywords
Design Methodology, Component Level Simulation, PSpice, MultiSim

1. Introduction

In terms of reducing design time, performance reliability, and overall practicality, circuit simulation platforms have garnered an important place in the IC design world. From anywhere between multinational semiconductor corporations to a startup business dealing with circuit design; it is conceivable that somewhere along the line it will incorporate a software based circuit simulation platform

in their course of action. The ability that these types of software can demonstrate and accomplish, specifically at design methodology and at component level simulation is what has made them so highly regarded and sought after. The focus here will be on two widely recognized simulation platforms; Orcad's PSpice and Electronic WorkBench's MultiSim. Specific case studies will be analyzed by both, and the ensuing results will be provided. It is worth mentioning here that the goal in this article is not to prove or endorse which platform is better, but simply to compare results we observe from both and discuss how each goes about their implementation. As stated in the above abstract, both analog and digital circuits will be used for simulation; although it will not be used in this article both simulation platforms also support mixed signal IC simulations. Lastly, an observation into the role that the higher abstraction languages, such as VHDL, can have in benefiting from these two simulation tools will be made.

Objective

To study and analyze circuit behaviour of specific case study circuit designs using simulations in PSpice and MultiSim. It is from these results(current and voltage transients, delays etc) that a basis will form in which to further provide a more informed conclusion as to their performance and futher involment in inplementation of higher level abstraction languages such as VHDL.

Methodologies

Provided here is a look at the test circuits. The first two are of the analog variety while the last two are simple digital circuits. The methodologies used are component level simulations using the PSpice and MultiSim with the same component values and also equivalent component parameters.

The following is an operational amplifier based integrator. Output Vo is the time integral of input V1. A function of the integrator is that it changes a square wave into a triangular wave, and a triangular wave into a sine wave, in this case the input is a square wave. The schematic of the design used is shown below in figure 1.

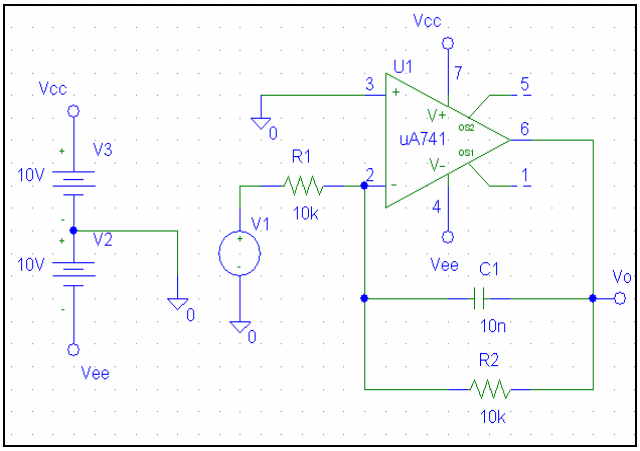

Figure 1: Integrator Circuit

The circuit, like all the other circuits presented in this article, was constructed and simulated in both platforms with same components, same values and behavior parameters. Although no step by step procedures will be presented, suffice it to state that different platforms have different attributes and in some cases differing interfaces, thus requiring some minor detailing to assure that a particular IC circuit simulation will be the same in PSpice as compared to MultiSim and vice versa.

The following results were obtained when simulating the circuit using PSpice. With PSpice, the resulting current and voltage transients can be obtained by either a graphical view such as the one in figure 2, or by viewing the resulting output file netlist. Here a graphical view is used in order to give a more visual(and simpler) illustration of the simulation. Although using a netlist will provide a very useful tool in the case in which other simulation tools, such as VHDL, is used.

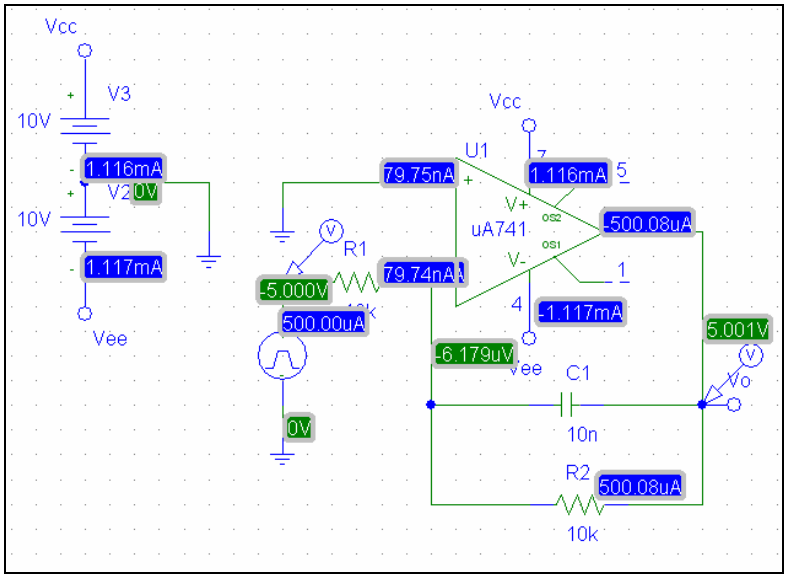

Figure 2: Current and Voltage Transients in PSpice

From these results, deduction of power distribution along the circuit can be gathered and analyzed. Next a transient analysis was performed. A square wave ranging between +/- 5 V, pulse width of 0.5 ms and a period of 1ms was placed at the input, and transient setup of 7ms with print step of 1ms was used. Figure 3 shows the resulting triangle wave with input square wave.

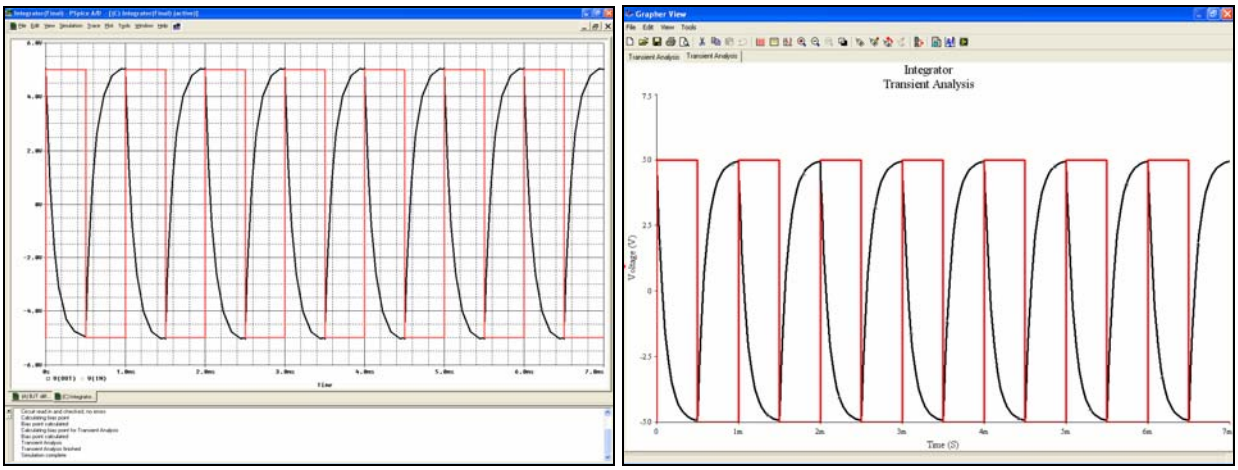

Figure 3: PSpice Transient Output

The left side of the figure corresponds to the PSpice transient analysis output. The right side corresponds to the transient analysis simulated in MultiSim.

A common BJT differential amplifier, such as the one in Figure 4 will be used for the last analysis of the analog portion of this article. For the sinusoidal input in the circuit the corresponding parameters were setup.

VOFF :0 V
VAMP: 1V
FREQ: 0.5kHz

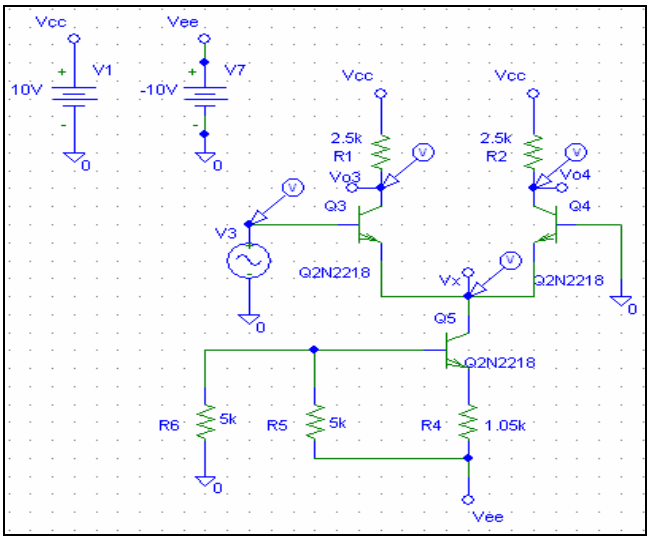

Figure 4: BJT Differential Amplifier

Using the PSpice simulation, the following results are displayed for voltage and current transients of the BJT differential amplifier, shown in figure 5.

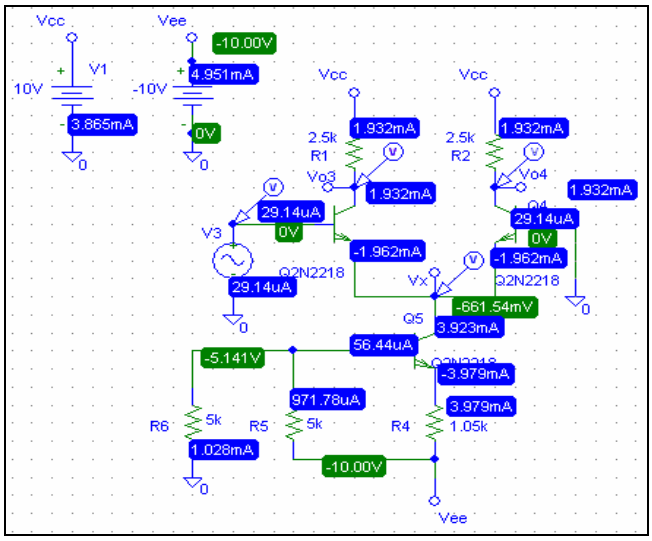

Figure 5: Current and Voltage Transients in PSpice

Using the MultiSim simulation, the following results for voltage and current transients of the BJT differential amplifier are shown in figure 6.

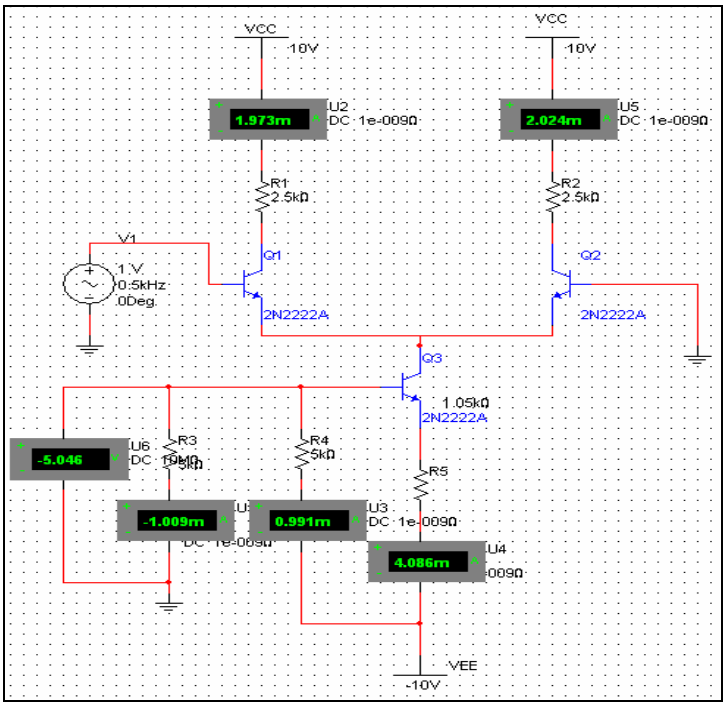

Figure 6: Current and Voltage Transients in MultiSim

Once again a deduction with regard to the voltage distribution in the circuit can be made by using the values shown in the current and voltage transients. Finally, the transient analysis is made at four points along the circuit using voltage markers in figure 5. The markers are placed at the input signal, and just above the common terminal of each of the transistors. Figure 7 shows the resulting transient analysis output for both platforms.

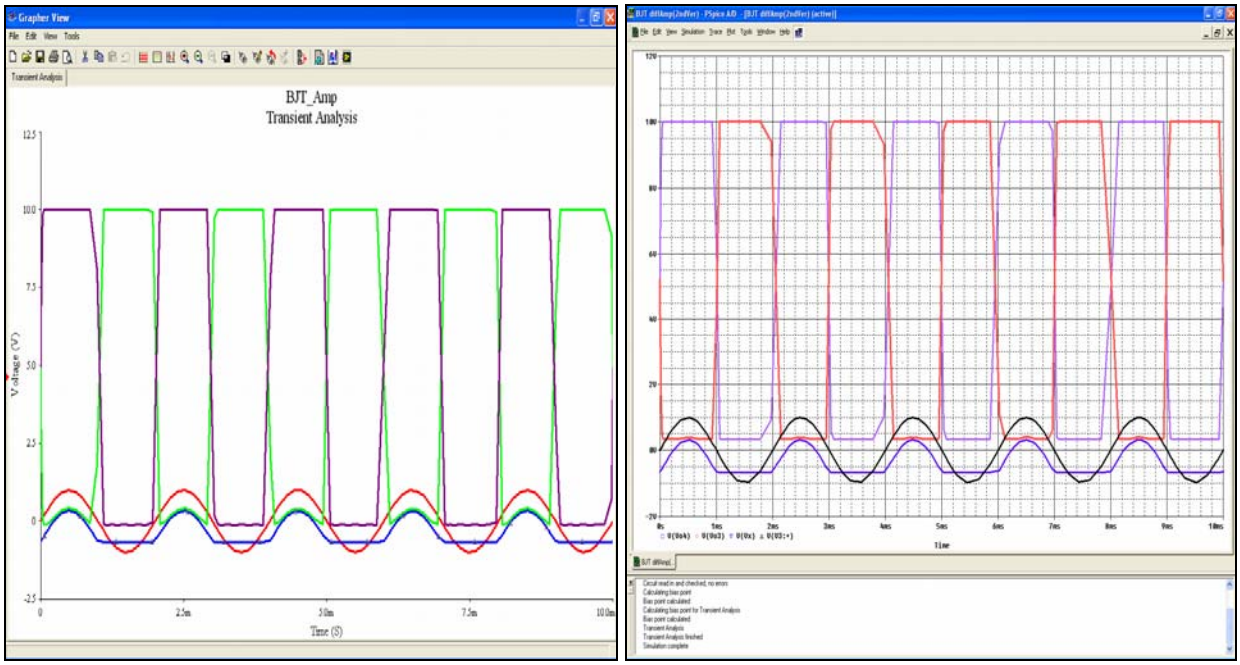

Figure 7: Transient Analysis of BJT Amplifier (L MultiSim; R PSpice)

Next, an examination will be made corresponding to the simulation of a simple digital circuit, in this case an XOR gate. Truth table for XOR is as follows:

Table 1: XOR Truth Table

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	0

Setting up the circuit in both platforms, the following results are obtained. Figure 8 shows a non-pulse input (manual inputs of hi (1) and low (0) states instead or a pulse wave of 0's and 1's), of an XOR gate with its corresponding output states.

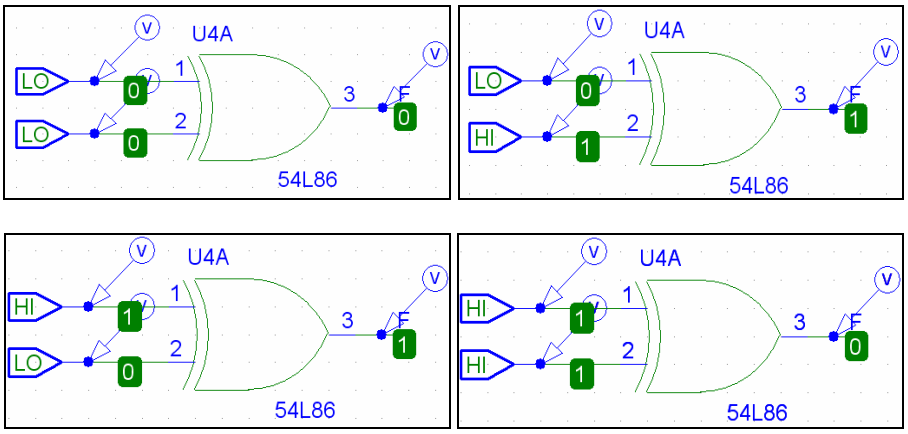

Figure 8: XOR Logic states in PSpice

MultiSim has a slight variation in the manner in which logic circuit states can be displayed. Figure 9 shows the XOR gate with its corresponding output results. Here the XOR gate is connected to inputs A and B of the Logic Converter (shown as part XLC1 in schematic below). Output is also connected to its corresponding output connection. From this information the Logic converter calculates a truth table from the corresponding inputs.

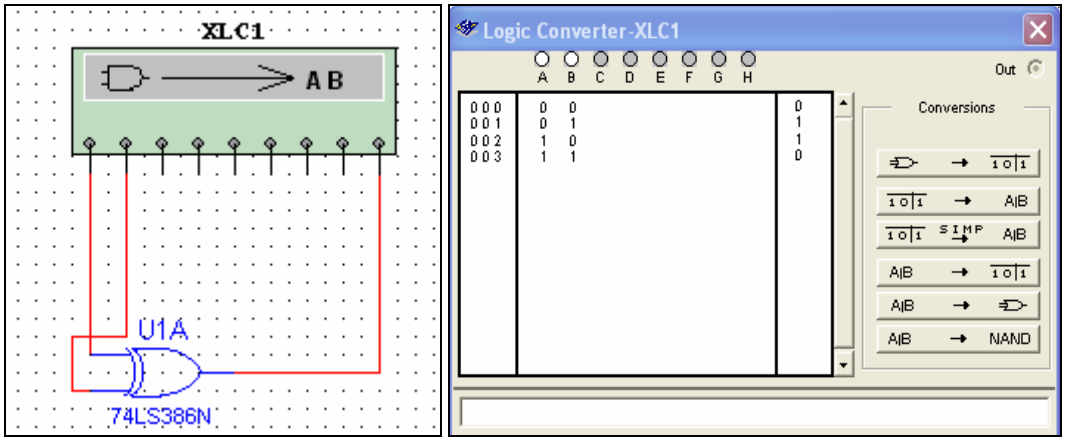

Figure 9: XOR Logic states in MultiSim

The last circuit used for simulation will be a 2-bit counter. The schematics shown below in figure 10 are for MultiSim and PSpice correspondingly.

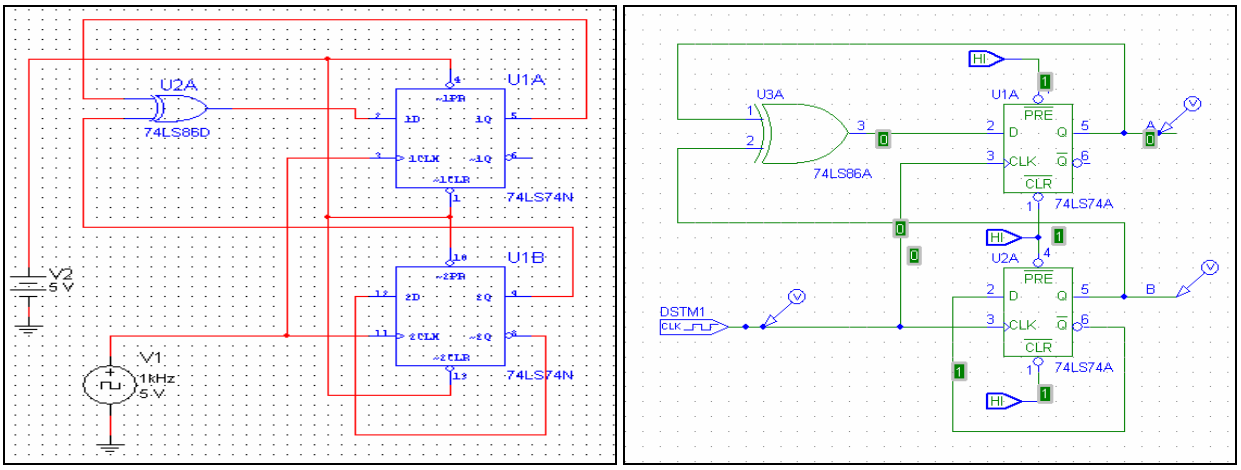

Figure 10: 2 Bit Counter schematic for MultiSim

Figure 11 shows the corresponding outputs of the 2 bit counter. The pulse input and resulting output waves are shown in both simulations. Left side of Figure 11 corresponds to MultiSim output and right side to the output in PSpice.

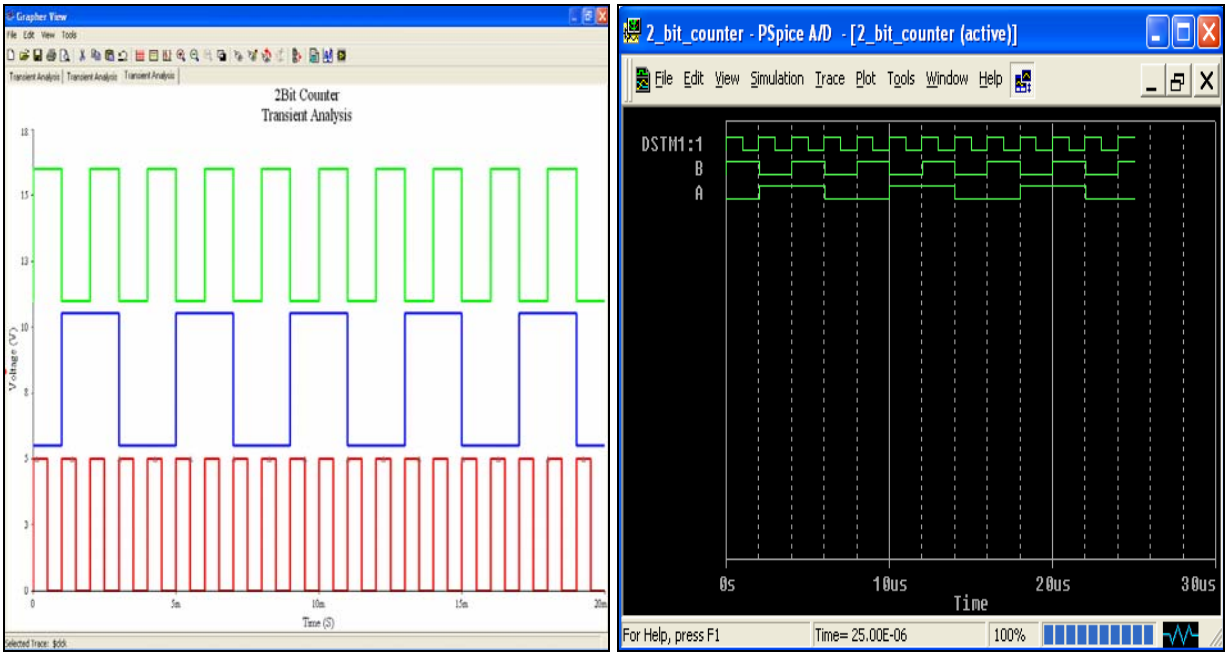

Figure 11 : Output of 2 Bit Counter

Finally, it is also worth noting that there exist a program called MutiHDL, which is in the same family of software products as MultiSim. Primarily used for digital circuits, MultiHDL is a HDL simulation program, that can be used to work alongside Spice models to simulate VHDL models. For instance the program can replace simple gates, at the schematic component simulation level, with VHDL models. It could also be used to simulate complex digital chips, creating simulation models for complex digital IC's

not normally modeled in SPICE simulations. Suffice this provides a nice interface scheme between itself and traditional simulation platforms, such as PSpice and MultiSim.

Conclusion

The main objective of this article was to study and analyze circuit behavior using two well known circuit simulation platforms; PSpice and MultiSim, and as a supplement how this in turn relates to higher level abstraction languages such as VHDL. It was shown in examples above that both perform at a high level in terms of ease of use, clear and concise displays and corresponding result outcomes. While maintaining their own interface schemes and subtle differences in certain circuit analyses, it should not be a deterrent for a PSpice user to simulate circuits in MultiSim and vice versa. Essentially, the learning curve for performing analysis in each of the platforms is minimal especially if the user has already been introduced and is knowledgeable regarding spice simulations. With regards to the VHDL component and related high level abtraction languages, we can only conclude given a circuit with a minimal to medium amount of complexity to it, traditional simultations packages are not only effective but efficient. It is true that given a circuit whose complexity is substancial, the use of netlist or descriptions such as those used in HDL's are easier to enter and follow than hundreds of thousands of individual interconnecting wires and in general reduce design-entry errors. Thus the relationship between the lower and higher abstraction languages does indeed hold a great deal of importance

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