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The System on Chip Technology

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Abstract

Increased developments in semiconductor processing technologies have made it possible to increase the density of gates in a silicon wafer according to what Moore's law had predicted so much so that a whole system can be fabricated on a single chip. SOC designs make available, on a single chip, embedded IP (Intellectual Property) and high-level integration required for performance and efficiency demanding applications. This technology called the System on Chip technology has resulted in lowering of cost of a particular system as opposed to its equivalent board level system. This paper describes the system on chip technology from the perspective of IP (Intellectual Property) core technologies, chalks out the advantages and disadvantages, provides information about the dilemmas and challenges faced by the SOC industry and suggests possible solutions and strategies. Details of applications, market trend, latest development in the field of SOCs like CSOCs (Configurable SOCs) and research in educational institutions have also been discussed.

Keywords
System-on-chip, challenges, solutions, applications, research in educational institutions

1. Introduction

Since a system built with standard parts requires more components than if the system were built with standard ICs designers tend to build smaller and simpler systems. There are standard parts available in the form of ICs for example gates, accelerators, floating point processors etc [4]. These standard ICs are used in systems resulting in reduction of cost and increased efficiency. Application Specific Integrated Circuits (ASICs) designers can create a single chip for a particular application. But with increased integration technology a complete system can be fabricated on a single chip. For example a computer fabricated on a single chip can include the processor, I/O devices and memory. Therefore system on chip is becoming increasingly popular in the field of embedded systems.

1.1Virtual Components and Design Reuse

The complexity involved in SOC designs invites a number of issues. This complexity has given rise to different terms like Virtual Components or Core and design reuse. One of the obvious problems faced by the System on Chip field is how to fit tremendous amount of logic into a single chip [3]. Not all the companies have the resources to develop all the Intellectual Property for a True System on Chip. Even those with the required knowledge and plentiful resources may still be unable to finish a complete chip design in time to meet accelerated market demands. This has resulted in design reuse where third party Intellectual Property is included in a design. Various companies focusing on SOC technology have encouraged cross licensing and technology sharing in order to take advantage of different IPs. But one problem that is faced is when a design is not fit for reuse. Therefore it has become highly important to develop a system with the reuse feature in mind. The term Virtual Component or Core actually denotes reusable semiconductor IP.

The virtual components may be hard with all the gates and interconnects placed and routed and all the silicon layers defined. Some may be soft with only the higher level register transfer language defined and some come as firm with some register transfer level description with some level of physical floor planning or placement but not the final routing.

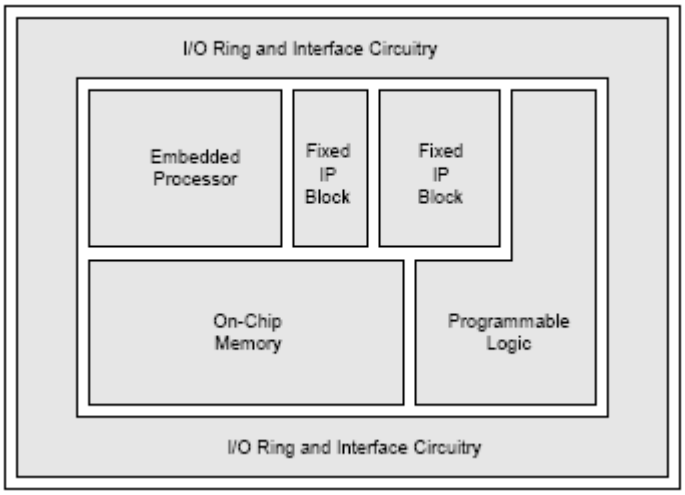

Figure: System on Chip design with fixed IP blocks [2]

2. Dilemmas and challenges faced by the SOC Industry

1) One of the Dilemmas faced by the System on Chip industry is that while the complexity of designs is increasing, the time to market is decreasing. The solution to this problem is evidently the use of reusable IP [3].
2) The other problem is that the integration function of SOC is being transferred. The ASIC Suppliers dilemma is that they do not usually have the virtual component expertise in all the diverse areas needed for a given SOC. The solution is to get the different virtual components from different divisions within the company or from third parties.

The term IP refers to the patents, trade secrets, design methodologies, trademarks of a design.

3) The third SOC dilemma is how to achieve reuse by mixing and matching third party and in house virtual components. Unlike individual chips on a printed circuit board, virtual components present a multitude of interoperability and integration challenges.
4) SOC designs concern themselves with the various electronic design automation tools, libraries and semiconductor processes of the different virtual components. SOC developers have to use several representation, environments and languages none of which are standard. There are also the few conversion tools between environments or languages.

To ease the use of design reuse and integration problems the Virtual Socket Interface Alliance was formed which promotes the development of technical standards required to mix and match virtual components from multiple sources. Fujitsu, Cadence and Toshiba formed the nucleus of the alliance which has now more than 200 members and this alliance focuses on more of technical issues focusing on problem of standard interfaces and data formats among virtual component block authors and SOC integrators[3], [5].

5) The challenges in SOC designs are the result of deep sub-micron complexities, testability issues and time to market pressures [6]. Wipro, a leading industry in embedded design services has provided five key aspects of a successful SOC design which are as follows [7]

    - Architecture Strategy: Something that defines SOC architecture is the kind of processor or core that one uses as the central processing element. For example, ARM processor core, MIPS core, PowerPC core etc. The application may necessitate the inclusion of DSP Cores in the design consideration.
    - Design for Test Strategy: In Wipro's SOC Flow most common physical defects are modeled as faults and necessary circuits are included in the design to facilitate checking for these faults.
    - Validation Strategy: When there are different functions integrated into a single chip, verification becomes a tedious task. The verification can be done at every stage of the design flow like RTL, gate level and post layout gate level with timing for successful verification of IP blocks.
    - Synthesis and Backend Strategy: As processing technologies move into deep sub micron levels physical effects like Electro Migration, IR Drop, Cross Talk and EMI effects become prominent. Therefore Chip Planning, Design for Test Planning, clocks planning and area budgeting at a very early stage is the core of the Backend Strategy
    - Integration Strategy where all the above aspects have to be bought together for a smooth design flow.

Different strategies, like these needs to be incorporated for improved performance and reduced overall system cost and to cope with the time to market pressures.

3. Advantages and Disadvantages of System on Chip

The advantages and disadvantages of System on Chip technology have been bought out by the way of comparison of board level systems and system on chip designs [8], [2]

3.1 Advantages of board level development

- Board-level debugging has the distinct advantage of visibility. When a particular board-level anomaly arises, the developer can physically modify the board by cutting traces, lifting pins, and adding wires.

- Board-level development enables individual devices to be replaced or upgraded. If a particular device goes bad, it's fairly easy to replace.
- Board-level debugging presents visibility to signals from the various components. The signals that travel from device to device are visible to analysis tools such as oscilloscopes, logic analyzers etc.

3.2 Disadvantages of board-level development

- Board-level systems with separate DSP and CPU often require different tool chains to support each device. Furthermore, the delineation of these devices makes CPU-DSP interaction problems difficult to resolve.
- Having a board with several discrete components can cause problems during the latter part of the support stage. As individual components become scarce or unavailable, finding replacement parts can be difficult. This may also result in software modifications to support the new "replacement" part

3.3 Advantages of SOC

- Hybrid CPU/DSP integrated devices are supported by the same tool chain. In some cases, the complier seamlessly weaves together code instructions for the CPU and DSP.
- Once a particular SOC is fully debugged and functional, the developer can be assured that all devices in the SOC work as documented. Furthermore, all of the signals have been pre-qualified, so we know that the device is operating properly. This in turn means that most of the problems encountered will be related to software.
- With highly integrated SOCs, hard cores can be used to implement highly computational functions in hardware.

3.4 Disadvantages of SOC

- Obviously, with this highly integrated device, you can't simply replace a particular device; you must replace the entire SOC. For example, if the CCD controller isn't working properly, you can continue to develop without CCD functionality. Otherwise you must replace the SOC itself
- Depending on the integrated device, you must be satisfied with how it was designed and integrated.
- Visibility into the SOC is limited.

The advantages and disadvantages clearly indicate the reason why System-On-Chip technology is the most sought after by industries dealing with embedded logic. By integrating multiple chips on a single silicon chip, and producing an all-in-one electronics product, companies expect to reap large benefits in terms of manufacturing, especially for markets where price and device size are of critical importance.

4. Research in educational Institutions

System on chip designs provide integrated solutions in the field of Telecommunications, multimedia, and consumer electronics domains. The system on chip field is pioneered by engineers, physicists, computer scientists, designers who need to develop methodologies, software, architectures, design tools etc which would provide the solutions to the existing dilemmas. This fact has opened research related to SOC design in educational institutions. Hardware and Software have to be co-designed in order to achieve successful integration of the IP blocks. This has led to exciting research opportunities in different educational institutions, some of which are listed below [9], [10], [11] and [12].

1) Rutgers, the State University of New Jersey has developed a research lab named WINLAB where wireless SOC is one of the focus areas.
2) At the Technische Universitat Darmstadt, Germany, Institute of Microelectronic systems offers a modern education in the area of microelectronics which will be able by the current improvements in the area of semiconductor-technologies to integrate complete systems on a single chip (Systems-on-the-Chip - SOC). The main areas of research are hardware software co-design, High Level Synthesis, Rapid Prototyping and Reconfigurable Architectures.
3) Canadian Microelectronics Corporation (CMC) has developed a software product to help university students and researchers create the next generation in microchip technology. With this the design flow is provided to the students already so that they can design the IP blocks for an SOC design. Using the uniform design flow will help the students to meet the industry standards and achieve successful IP integration.
4) The University of Texas at Austin and IBM Research, based on support from the Defense Advanced Research Projects Agency (DARPA), will collaborate to produce an adaptive, high-performance microprocessor that could revolutionize computing. The university team has conceived a new architecture, called TRIPS (Tera-op Reliable Intelligently-adaptive Processing System), that is designed to provide supercomputer performance on a single chip. Researchers at IBM's Austin Research Lab are working closely with The University of Texas at Austin team to develop a number of the relevant technology innovations necessary to realize such systems, and engagements are underway to ultimately commercialize the results.
5) The Electronics System Design Research Group in Loughborough University, UK has focused their research of System on Chip technology in Real Time Embedded Applications as well as development methodologies to achieve efficient performance.

5. Conclusion

Despite the numerous challenges that the System-On-Chip field is facing, this technology will continue to grow. The collaboration of universities with industry will definitely give rise to exciting research that will help the growth of this field and will also help solve the challenges that are faced by this field. With increasing time to market pressures, FPGAs, Programmable logic devices and complex programmable logic devices will be merged into SOCs. The recent advances in the technology namely Configurable System on Chip CSOC, will increase tremendously the SOC Market. CSOCs satisfy the time to market pressures with providing the programmable capability of a PLD.

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